IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An interconnect comprising:

a trench including a first barrier layer and a seed layer, the trench having a depth and a width, the depth being greater than a critical depth; and

at least one metal layer above the seed layer; ~~a number of metal layers above the trench,~~

wherein the number of metal layers is determined by the width and wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

2. (Canceled)

3. (Currently Amended) The interconnect of claim 1, wherein at least one of the ~~number of~~ metal layers is fabricated from copper.

4. (Currently Amended) An interconnect comprising:

a trench including a first barrier layer and a seed layer, the trench having a width and a depth, the depth being greater than a critical depth;

a number of metal stack layers capable of defining a critical width and located above the trench; and

a number of metal layers above the trench, wherein the number of metal layers above the trench is a function of the width and the critical width;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer; and

wherein the critical width includes twice the sum of the first barrier layer sidewall thickness and the seed layer sidewall thickness and the metal layer sidewall thickness.

5. (Original) The interconnect of claim 4, wherein the width is greater than the critical width.

6. (Original) The interconnect of claim 4, wherein each of the number of metal stack layers is planarized by chemical mechanical polishing.

7. (Currently Amended) An interconnect comprising:

a trench including a first barrier layer and a seed layer, the trench having a depth and a width; and

a number of metal layers above the trench, wherein for the depth being greater than a critical depth, the number of metal layers are capable of being increased as the width increases, and wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

8. (Currently Amended) An interconnect comprising:

a trench including a first barrier layer and a seed layer, the trench having a trench depth greater than a critical depth;

a number of metal stack layers above the trench, the number of metal stack layers having a thickness; and

a number of metal layers above the trench, wherein the number of metal layers is capable of being increased as the thickness decreases;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

9. (Original) The interconnect of claim 8, wherein at least one of the number of metal stack layers above the trench couples a first logic device to a second logic device.

10. (Currently Amended) An interconnect comprising:

a first memory cell;

a second memory cell;

a trench including a first barrier layer and a seed layer, the trench having a trench depth greater than a critical depth; and

a number of metal stack layers above the trench, wherein each of the number of metal stack layers has a sidewall thickness, the number of metal stack layers above the trench is capable of being increased as the sidewall thickness decreases, and at least one of the number of metal stack layers couples the first memory cell to the second memory cell;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

11. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer and a seed layer, the first trench having a depth greater than a critical depth and a width less than twice a first sidewall thickness;

a second trench including the first barrier layer and the seed layer, the second trench having the depth of the first trench and a width greater than twice the first sidewall thickness and less than twice a sum of the first sidewall thickness and a second sidewall thickness;

a first metal layer above the first trench and the second trench; and

a second metal layer above the second trench;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

12. (Original) The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a memory module.

13. (Original) The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a logic module.

14. (Canceled)

15. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer and a seed layer, the first trench having a top and a depth greater than a critical depth, and a width less than a sidewall width of a first metal;

a second trench including the first barrier layer and the seed layer, the second trench having a depth greater than ~~a second~~ the critical depth, and a width greater than twice the sidewall width of the first barrier layer and the seed layer and the first metal, and less than twice a sidewall width of a second metal; and

a first and a second metal deposited on the first trench and the second trench, the second metal is planarized to the top of the first trench.

16. (Original) The interconnect of claim 15, wherein the second metal comprises Al.

17. (Original) The interconnect of claim 15, wherein the second metal is planarized by chemical mechanical polishing.

18-22. (Canceled)

23. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer and a seed layer, the first trench having a width and a metal layer; and

a second trench having a depth greater than a critical depth and a second width greater than the width, the second trench having a plurality of metal layers and at least one of the plurality of metal layers is coupled to the metal layer;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a first metal layer of the plurality of metal layers and a vertical thickness of a second barrier layer.

24. (Original) The interconnect of claim 23, further comprising a wire bond coupling a conductive material to at least one of the plurality of metal layers.

25. (Original) The interconnect of claim 24, wherein at least one of the plurality of metal layers is aluminum.

26. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer and a seed layer and a copper layer, the first trench having a depth greater than a critical depth ~~and a copper layer~~; and

a second trench wider than the trench, and the second trench including the first barrier layer and the seed layer and the copper layer and having a plurality of metal layers, wherein at least one of the plurality of layers is an aluminum layer, and at least one of the plurality of metal layers is coupled to the copper layer;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer.

27. (Original) The interconnect of claim 26, wherein the aluminum layer is an aluminum alloy layer.

28. (Currently Amended) The interconnect of claim 26, wherein at least one of the plurality of metal layers is a copper alloy layer.

29. (Original) The interconnect of claim 26, wherein the aluminum layer is wire-bonded to a conductive material.

30. (Original) The interconnect of claim 29, wherein the conductive material is gold.

31-47. (Canceled)

48. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer and a seed layer, the first trench having a depth less than a critical depth and a width less than a critical width and a metal layer; and

a second trench having a depth greater than [[a]] the critical depth;

a plurality of metal layers above the second trench, at least one of the plurality of metal layers is coupled to the metal layer, wherein at least one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a conductive material;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of a metal layer and a vertical thickness of a second barrier layer, and wherein the critical width includes twice the sum of the first barrier layer sidewall thickness and the seed layer sidewall thickness and the metal layer sidewall thickness.

49. (Original) The interconnect of claim 48, wherein the metal layer is copper.

50. (Currently Amended) The interconnect of claim 49, wherein at least one of the plurality of metal layers is aluminum.

51. (Original) The interconnect of claim 48, wherein at least one of the plurality of metal layers is an aluminum alloy.

52. (Currently Amended) An interconnect comprising:

a first trench including a first barrier layer, a seed layer, ~~having~~ and a metal layer, the first trench ~~and~~ having a depth greater than a critical depth; ~~and~~

a second trench including the first barrier layer and the seed layer and having a plurality of metal layers, at least one of the plurality of metal layers is coupled to the metal layer, wherein

only one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a gold wire; and

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of the metal layer and a vertical thickness of a second barrier layer.

53. (Original) The interconnect of claim 52, wherein the second trench has a depth greater than the critical depth.

54. (Currently Amended) A conductive structure comprising:

a first trench including a first barrier layer, a seed layer, and a metal layer and having a width, and a depth~~, and a metal layer~~; and

a second trench including the first barrier layer and the seed layer and having a width, a depth, and a plurality of metal layers, the width of the second trench is greater than the width of the first trench, and at least one of the plurality of the metal layers is electrically coupled to the metal layer.

55-56. (Canceled)

57. (Currently Amended) A conductive structure comprising:

a narrow trench including a first barrier layer, a seed layer and having a metal layer and a depth greater than a critical depth; and

a wide trench having a plurality of metal layers and a second depth equal to the depth, wherein at least one of the plurality of metal layers is coupled to the metal layer;

wherein the critical depth includes a vertical thickness of the first barrier layer and a vertical thickness of the seed layer and a vertical thickness of the metal layer and a vertical thickness of a second barrier layer.

58. (Currently Amended) An interconnect comprising:

a trench including a first barrier layer and a seed layer and having a width less than a critical width, a depth and a metal layer; and

a wide depression having a second width greater than the critical width, a second depth equal to the depth, and a plurality of metal layers, wherein at least one of the plurality of metal layers is coupled to the metal layer;

wherein the critical width includes twice the sum of the first barrier layer sidewall thickness and the seed layer sidewall thickness and the metal layer sidewall thickness.

59-80. (Canceled)